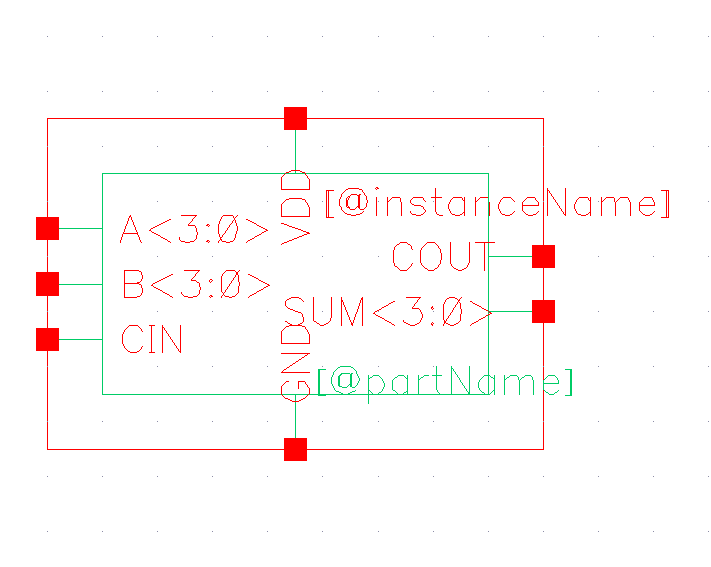
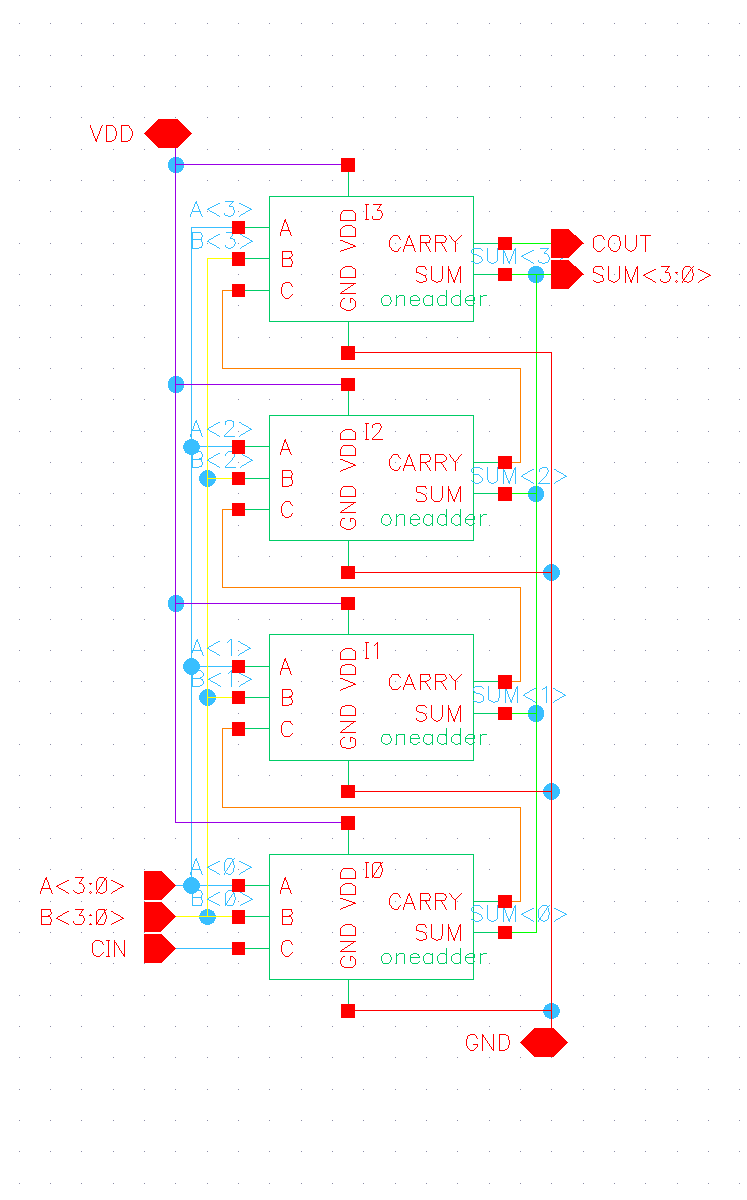
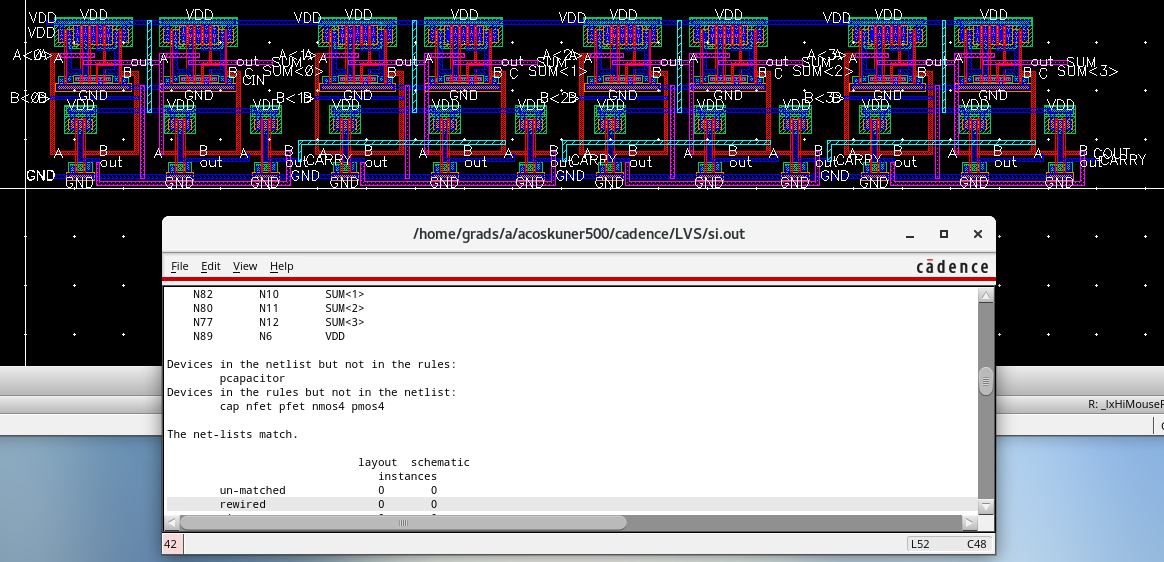
**ECEN 714-612 Lab 5**

1. 4-bit Adder (Schematic, Layout, LVS)





1. Simulation

Expected vs Actual

| **Expected** | | | | | **Actual** | |
| --- | --- | --- | --- | --- | --- | --- |
| **A<3:0>** | **B<3:0>** | **Cin** | **Cout** | **SUM<3:0>** | **Cout** | **SUM<3:0>** |
| 0000 | 1111 | 1 | 1 | 0000 | 1 | 0000 |
| 1010 | 0101 | 0 | 0 | 1111 | 0 | 1111 |
| 1010 | 0101 | 1 | 1 | 0000 | 1 | 0000 |
| 1100 | 1000 | 0 | 1 | 0100 | 1 | 0100 |

Delay and VDD Power

|  | **Cout** | **SUM<3>** | **SUM<2>** | **SUM<1>** | **SUM<0>** | **VDD Power** |
| --- | --- | --- | --- | --- | --- | --- |
| 0000+ 1111+1 | 1.163E-9 | 1.166E-9 | 924.0E-12 | 682.4E-12 | 436.4E-12 | -63.11E-6 |
| 1010+ 0101+0 | 931.4E-12 | 964.2E-12 | 757.7E-12 | 551.8E-12 | 352.8E-12 | -113.8E-6 |
| 1010+ 0101+1 | 1.163E-9 | 1.166E-9 | 924.0E-12 | 682.4E-12 | 438.6E-12 | -63.35E-6 |
| 1100+ 1000+0 | 456.0E-12 | 863.0E-12 | 532.4E-12 | 652.4E-12 | 481.1E-12 | -88.94E-6 |



